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UNIT
FINAL REPORT
8 MARCH 1976

Prepared by:

Teledyne Controls 200 North Aviation Boulevard El Segundo, California 90245



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Approved:

Project Engineer

ABSTRACT

NASA Contract NAS 9-13565 was awarded for laboratory hardware to evaluate Shuttle instrumentation, data processing and ground check-out operations. This document briefly describes the design and testing of the hardware required for this evaluation.

The hardware was a modification of a somewhat similar instrumentation system. A Data Bus Coupler was designed and tested to interface the equipment to a central bus controller (computer). A Serial Digital Data transfer mechanism was also designed. Redundant power supplies and "overhead modules" were provided to minimize the probability of a single component failure causing a catastrophic failure. The unit was packaged in a modular configuration to allow maximum user flexibility in configuring a system.

Test procedures and special test equipment for use in testing the hardware were provided.

The units were delivered to NASA and appear to be adequately performing their intended function.

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LIST OF ABBREVIATIONS

A list of abbreviations is included in the table below to aid the reader of this report:

Abbreviation	Description
ADC	Analog/Digital Converter
ADP-M	Analog Data Processor Module
AIFTDS	Airborne Integrated Flight Test Data System
AMX	Analog Multiplexer
AOC	Analog Output Card
BITE	Built In Test Equipment
CAL	Calibration
CDU	Command Decoder Unit
db	decibel
DBC	Data Bus Coupler
DCB	DC Bridge
DDP-M	Digital Data Processor Module
DMX	Discrete Multiplexer Card
DOC	Discrete Output Card
GPA	Gain Programmable Amplifier
1/0	Input/Output
LLC	Low Level Calibration
MHz	Megahertz
PCM	Pulse Code Modulation
PTP	Production Test Procedure
RMDU	Remote Multiplexer/ Demultiplexer Unit

LIST OF ABBREVIATIONS

(Continued)

Abbreviation	Description
SDI	Serial Digital Interface
PTP	Production Test Procedure
SD I/O	Serial Digital Input/Output
SPS	Samples Per Second
TTL	Transistor - Transistor Logic

INTRODUCTION

Teledyne Controls entered into a contract with NASA-JSC on 6/25/73. This contract, NAS9-13565, was for a design study to clarify certain Shuttle requirements and for the design and development of a Command Decoder Unit (CDU) for use as a Shuttle compatible data acquisition/command decoder remote terminal. This unit was to be used in the evaluation of techniques for implementing operational instrumentation, data processing and ground checkout operations.

The CDU was to be designed to provide, to the greatest extent possible, the following:

- 1.) Maximum Shuttle compatibility.
- 2.) A data bus terminal which is configurable, via the use of a basic set of plug-in interface modules, to satisfy various data acquisition and command stimuli requirements of the Shuttle avionics subsystems.
- 3.) A basic set of subsystem interface modules which provide input/output signal conditioning to satisfy subsystem sensor interface requirements.
- 4.) A data bus transmission system design which satisfies the data transfer requirements of Shuttle instrumentation, data processing and ground checkout systems.
- 5.) A design using off-the-shelf hardware where possible.

The following background information was provided:

"The Space Shuttle data processing and instrumentation subsystems utilize remote data terminals to both acquire data from and distribute data to vehicle subsystems for flight control, performance monitoring and recording, pre-launch checkout, and other functions. These terminals both receive and respond to commands sent from the controlling system hardware (avionics computers, PCM telemetry equipment, ground checkout computers) over serial data busses. These data busses substantially reduce vehicle wiring by utilizing time division multiplexing and pulse code modulation techniques to transfer data between the remote terminals and the command generators.

The advantages of using common hardware elements for implementation of these remote terminals is obvious and the concept of using remote terminal equipment, which is configurable to meet the specific input/output requirements of any subsystem interface, has been proposed for the Shuttle. The availability of system elements capable of meeting these goals should be determined and a typical system comprised of these units acquired for integration into the Shuttle Avionics Integration Laboratory. This will allow evaluation of these units prior to the finalization of the Shuttle Avionics design, and identification of the modifications required to adapt these units to the Shuttle."

DESIGN STUDIES

The design studies outlined in the original contract called for the development of alternative approaches or concepts and an evaluation of the feasibility of these approaches. Preliminary specifications were to be prepared incorporating the chosen approaches.

The basic CDU requirements, as defined in section 3.3.1 of the NASA Statement of Work dated January 19, 1973, were expanded and updated

to incorporate existing hardware specifications where this was found to be the most satisfactory approach. The Data Bus Coupler (DBC) and the Serial Digital Input/Output (SD I/O) requirements were updated to incorporate the design study results, latest Shuttle requirements and NASA-JSC recommendations. This change was incorporated into the contract as part of Change No. 2 dated 8 November 1973, which also deleted most of the formal design study reporting requirements.

Two design study reports were submitted to NASA as required by contract Change No. 2. These were "A Data Bus Coupler Design" and "A Serial Input/Output Mechanication." The results of both of these study documents were reflected in the delivered hardware.

The first report, "A Data Bus Coupler Design", outlines the DBC requirements, defines the data bus and then presents the design that resulted after an extensive period of breadboarding and laboratory evaluation.

Probably the most important part of the DBC design was the receiver input circuitry. Here, a balanced transformer-coupled input was used followed by a pair of symmetrical hot carrier diode clippers. A series resistor-capacitor network was used between transformer secondary and the diode pair. The capacitor value was chosen to be approximately equal to the diode capacitance, further improving noise performance under weak signal conditions. The output from the diode clipper was amplified by a high gain high slew rate operational amplifier, filtered by a low-pass filter and again passed through a symmetrical clipper. This processing caused any transitions to appear as short duration signals, minimizing detection circuitry interference by noise.

Breadboard tests were performed on the receiver circuitry and an error rate of less than 1 in 10⁸ was detected while operating with a 14 db signal to noise ratio using 0 - 4 MHz bandwidth gaussian noise.

The report included a Data Bus Coupler Specification in Appendix "A".

Assembly drawings, schematics and interconnect drawings were included in Appendix "B".

The second report, "A Serial Input/Output Mechanization" defined a means of acquiring or disseminating serial digital data over dedicated lines. The approach used in this report took advantage of most of the circuitry developed for use in the DBC. Because several Serial I/O Modules could be used in a single CDU, the serial channel implementation used two separate modules. One module contained the common circuitry and the second module was designed as a four channel multiplexer for the first one. The same transformers, receiver circuitry and sync detection circuitry as used in the DBC are used in this design.

Interface signals are defined. Timing diagrams, block diagrams and detailed theory of operation are included in the report. Schematics, outline and Assembly drawings are included in Appendix "A".

CDU DESIGN AND DEVELOPMENT

General

The CDU specification, as incorporated by Change No. 2 dated 8

November 1973, defined a unit which contained removable Input/Output
(I/O) modules. A basic CDU housing with associated power supply,

Data Bus Coupler and various other "overhead" modules could be operated as a single unit or it could be operated back-to-back in a fully

redundant mode. See Figure 1 for a simplified block diagram. Each side of the redundant CDU could be controlled via its own DBC module and, as such, could control the I/O modules in both sides.

Input/Output Cards

The basic I/O modules and the module addressing scheme were taken from an existing Teledyne AIFTDS-4000 Remote Multiplexer/Demultiplexer Unit (RMDU) design. The Analog Multiplexer Card (AMX) and the D.C. Bridge Multiplexer Card (DC BRIDGE) designs were used without redesign.

The Analog Output Card (AOC) design was modified slightly by addition of C-MOS data registers to prevent loss of data during short duration power interruptions. The analog output buffers were also improved by adding current limiting and overvoltage protection.

The Discrete Multiplexer Cards (DMX) were modified by the addition of optical isolators and a floating power supply to provide floating inputs. C-MOS storage registers we also added to these units to provide memory during short power interruptions.

The Discrete Output Cards (DOC) were designed for the Shuttle requirements. The card addressing philosophy was already established for the other cards. The new design effort involved taking the two stored 16 bit digital words and providing an individual floating solid state switch contact for each bit. Two types of units were required - one for use in 5 volt applications where the switch would interface with TTL logic and the other for use in switching 28 volt DC loads. Optical couplers were used in each design to provide D.C. isolation. An isolated 6 VDC supply was used to provide power to the output circuitry in the

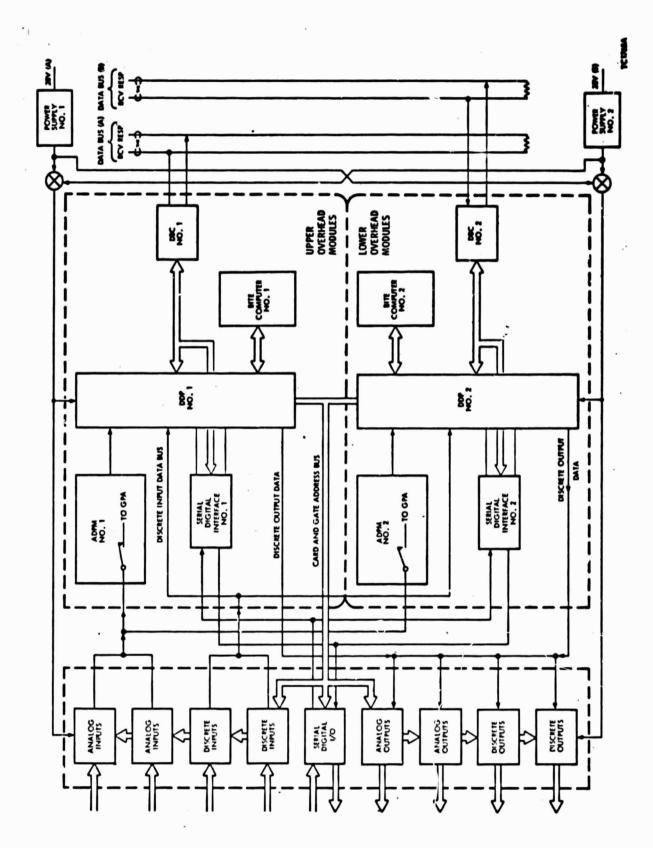


Figure 1. CDU Block Diagram

TTL-compatible circuit. The 28 volt output switch is powered from an external power source so additional isolated power was not required. These circuits were packaged as the 5 volt DOC, Part No. 839500, and the 28 volt DOC. Part No. 839503, respectively.

The Serial Input/Output card was designed in accordance with the second design study report. It used receiver and transmitter transformers that were designed for the Data Bus Coupler. The circuitry for use in driving the dedicated lines was also the same as used in the DBC. The Serial I/O was packaged in a standard I/O card configuration. It is addressed as a four channel input-output multiplexer for the Serial Digital Interface (SDI) Module in the CDU "overhead" section.

Overhead Modules

Referring back to Figure 1, the "overhead" modules are the ADP-M, DDP-M, DBC, BITE Computer, Serial Digital Interface Module and the Power Supply. These modules are required to operate any combination of up to 16 I/O modules. They were designed and packaged in a modular housing. Each "overhead" module is packaged as a removable assembly to simplify troubleshooting and maintenance. Identical overhead modules are used in each half of the redundant CDU housing.

The Analog Data Processor Module (ADP-M) was similar to the unit being used in the Teledyre RMDU. The unit was re-packaged on a slightly larger printed wiring card to be compatible with the other cards in the CDU. A small reed relay was added in series with the analog data bus to physically disconnect the card from the analog bus when the card is not in use. This was done to prevent a shorted input on one ADP-M from disabling the entire CDU by shorting out all analog data.

The Digital Data Processor Module (DDP-M) was designed to interface with the DBC and convert data bus address information into CDU card slot, channel address and ADP-M gain. The card slot, channel address format and ADP-M gain format was taken from the existing Teledyne RMDU design. Erasable E-PROMS were used to store the table of card and channel addresses for each DBC line address. The unit was designed, breadboarded and tested as part of this contract. The final circuitry was packaged on the appropriate size printed circuit cards for use in the CDU.

The DBC was designed and tested as defined in the first study report.

The completed circuitry was packaged on four printed circuit cards.

One card was used as the main connection to the CDU and all other cards were then interconnected via Kapton coated flexible printed wiring cables. All cards were fastened together to form a single plugin module.

The BITE Computer was designed for use in the CDU. It is a special purpose digital computer capable of performing real time in-flight tests and does not require initiation by the computer. It generates the CAL/BITE channel address and the proper gain where required, stores the Hi/Lo limits for the selected CAL/BITE data, tests itself and stores the results. The contents of the BITE Status Register are available to the computer by request via the DBC. The BITE Bit assignments are shown in Table 1.

BB5 to BB20 are from the low level calibration (LLC) of each analog input card so each bit indicates whether the corresponding LLC is within the specified tolerance. These bits are summed through 16 input NAND gates. If any one of 16 I/O cards fail, binary level "1"

Table 1
BITE Bit Assignments

			eignmente in					BITE Status Register Format
ВВ	2 3	HLC	er Supply BIT	E Statue	Ε.	Bit	1 2	Power Supply BITE Status
	4		-Ø, X512				3	GPA-0, X1
	5	LLC	Card Slot				:	GPA-Ø, X512
	6						?	Non-Existing Address Request (NEA)
	7	1		1			٠	Power Up/Down #1 (PU 1)
	8	1		V				Power Up/Down #2 (PU 2)
	9		. 5					Validity Low Level Cal/BITE Status
	10			1			10	TBD
	11	1	7				ii	
	12	1	8	1			12	ì
	13	- :	9				13	i .
	.14		10				14	i
	15	- 1	11				15	. 1
	16	1	12			Bit	16	TBD
	17	. :	. 13					
	18	ı	14			 		and the second s
	19		15			a.		*
BB	20	LLC,	Card Slot 16					

appears at bit 9 in the BITE Status Register. This information is then sent to the computer as part of the BITE status word.

The unit was designed with electrically programmable silicon gate MOS (E-PROM) memory devices. These are used to store high-low limits for the various parameters being checked by the BITE Computer. They may be erased and the limits changed in approximately 2 minutes. The procedure was outlined in the CDU Operation and Maintenance Manual.

The BITE Computer was packaged as a two card module. The first card connects to the CDU via a 160 pin connector and contains all memory devices. The second card is installed behind the first and connects to it by use of a Kapton printed wiring cable. The cards are fastened together to form a single module.

The Serial Digital Interface Module (SDI) was designed and tested as defined in the second study report. The SDI circuitry was taken from the DBC design where functional requirements were compatible. The entire input-sync detection section was used from the DBC and the output driver circuitry was also found satisfactory.

The completed unit was packaged in a two card module where one card was fitted with a 160 pin connector to connect to the CDU wiring and the second card was connected by Kapton cable to the first. When bolted together, the unit becomes a single removable module.

The CDU operates from two separate power busses when in the redundant mode. The unit must function properly if either power bus fails. Therefore, a separate power supply is provided in each half of the redundant CDU. The power supply was designed to meet the redundancy and fault-isolation requirements of the CDU specification. When both power busses are being used, the outputs of the two supplies are in parallel. Both supplies are then synchronized from the same external clock.

Each power supply consists of two sections, an inverter assembly and a regulator assembly. The inverter section contains the transistorized chopper, power transformers and rectifier circuitry required to generate the DC voltages necessary to operate the CDU. The regulator portion contains a synchronous pulse width regulator designed to efficiently produce a regulated DC voltage capable of powering a transistorized inverter. The overall supply consists of a case containing two plug-in printed wiring cards and a separate heat sink assembly which connects to the rest of the power supply by separate cable. This heat sink assembly contains chopper transistors and series regulator switch. A printed wiring board is attached to the assembly and contains the associated circuitry.

A considerable amount of system check-out time was required to identify and eliminate power supply switching transient noise that caused errors in the sample-and-hold circuitry and the analog to digital converter on the ADP-M. It became necessary to inhibit both regulator and chopper switching during the analog conversion time. It was also found that the transformers and other magnetics were easily saturated due to unsymmetrical waveforms caused by simply inhibiting the switching process during conversion. In order to prevent this problem, an UP-DOWN Counter was used to count the 4 MHz CDU clock. When the power supply clock is inhibited for an analog conversion, the counter counts up once for each pulse received. After conversion and the first transition, the counter must count down to zero before the power supply resumes its normal operation. Thus, a single symmetrical cycle of a longer period has been produced by the chopper and no transitions took place during analog conversion. This solved the noise problems in the CDU and all units were modified to include this circuitry.

The power supply was designed with a minimum of filtering in the basic power supply. Additionally, ceramic capacitors were used to minimize the probability of catastrophic shorts. Most of the filtering was placed on each individual circuit card where a fuse was installed between tantalum capacitor and the power supply. In this way, should a filter short or a catastrophic short occur on any card, the fuse would blow, clearing the voltage bus.

It was found that the above filtering approach allowed excessive transients in certain power supply lines. Also, as I/O card complements were changed, the amount of card filtering increased or decreased, changing the ripple on some supply voltages. In order to reduce the above problems, 1 Uf ceramic capacitors were installed in each half

of the CDU on a terminal board (TB1) in the main housing where the flexible cables and bus bars were connected to the power supply connector wiring. This added sufficient capacity to reduce noise pick-up on the flexible cables and helped to reduce ripple variations. Overall performance and analog stability in particular were improved by this change. All units were modified by addition of this filtering.

Packaging

The CDU packaging approach is best understood by referring to Figure 2, an exploded view of the CDU. Each half of the overall redundant CDU contains individual plug-in modules. The first eight card slots behind the front panel connectors are for Input/Output cards. Each card slot has a dedicated connector on the front panel and will accept any of the different types of I/O modules. The Data Bus Coupler and the other "overhead" modules are installed in their respective slots behind the I/O cards. The power supply is mounted in a shielded compartment at the rear of the unit. Printed wiring cables and heavy bus bars run the full length of the card connectors and provide all intercard connections. In the redundant mode, control signals, power supply outputs, etc., are properly connected via interface connectors in the base of each unit. A photograph of the completed CDU is shown in Figure 3.

Testing

A test plan was prepared and submitted to NASA for review, as required. Production test procedures and production test fixtures were prepared to provide uniform testing of the various modules. A system Acceptance Test Procedure was also generated and submitted to NASA. All five CDU's were tested in accordance with this test procedure. A test report was prepared and submitted for each individual unit that was shipped, by serial number.

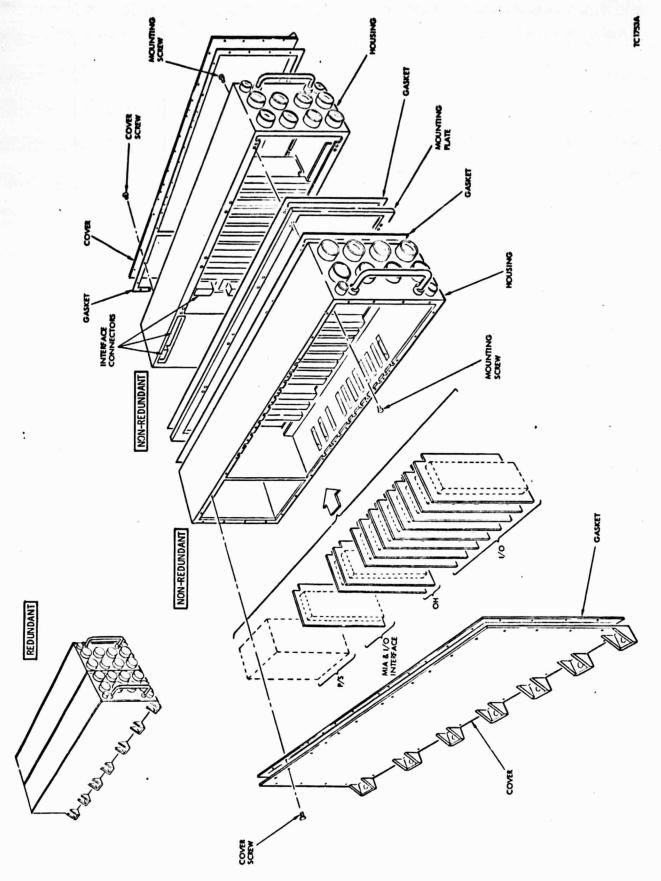


Figure 2. Exploded View of CDU

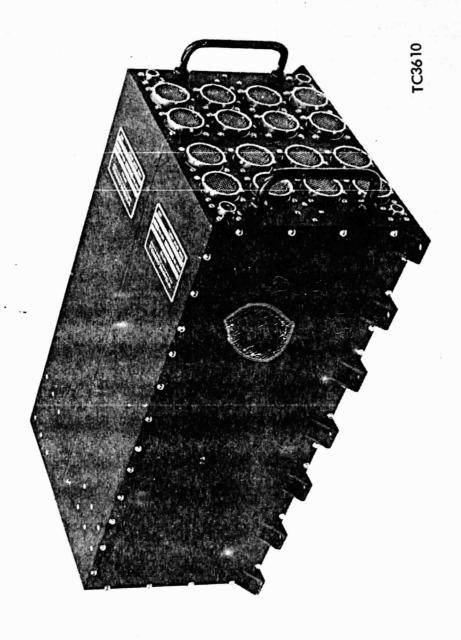


Figure 3. The Command Decoder Unit

Special Test Equipment

Two pieces of special test equipment were designed and assembled for use in the system testing of the CDU. A Data Bus Coupler test set (Teledyne Part No. 839753) was designed to exercise the DBC and the Serial Digital Input/Output cards. The tester could generate all the necessary commands, receive and store the responses from the DBC and detect various message errors. An operators manual was prepared. It contained schematics, copies of the various test procedures which require use of the test set and a brief theory of operation section.

The second piece of special test equipment was a Special Stimulus Test Set (Teledyne Part No. 840520). This was capable of exercising each type of I/O module. An operators manual was also prepared for this unit.

Both of these pieces of special test equipment were retained at Teledyne for use in testing CDU's on NASA Contract NAS9-13813, which was for additional CDU's. A 300 foot data bus simulator (Teledyne Part No. 839929) was also built and used for system tests. It was also retained for use on the second contract.

Documentation

An Operation and Maintenance Manual was prepared under this contract for the CDU. The manual was divided into two volumes. Volume 1 contains information relative to the basic CDU. It covers the housing, power supply and all "overhead" modules. A brief chapter on field repair and maintenance is also included. Complete schematics, test procedures, lists of materials and outline and assembly drawings are included for each module. A description, theory of operation and repair or troubleshooting procedure are included for each item.

The second volume contains complete information as outlined above for all Input/Output modules. The design specifications are also included for each of these modules.

These manuals were delivered to NASA as required in the contract.

Other documentation such as monthly reports, design review packages, etc. were also prepared and delivered as required during this contract period.

Recommendations

The CDU is a redundant modular remote terminal which may be configured to meet a wide variety of specific input/output requirements. It interfaces with the data bus via a DBC which is compatible with Shuttle hardware. The unit should allow NASA to evaluate various system combinations and develop software for future applications. It is felt that the present unit is capable of meeting all these requirements without modification. The unit should be re-packaged if it becomes necessary to subject it to a full flight environment.